



TSH150

WIDE BANDWIDTH AND BIPOLAR INPUTS SINGLE OPERATIONAL AMPLIFIER

- LOW DISTORTION
- GAIN BANDWIDTH PRODUCT : 150MHz
- UNITY GAIN STABLE
- SLEW RATE : 190V/ μ s
- VERY FAST SETTLING TIME : 20ns (0.1%)

DESCRIPTION

The TSH150 is a wideband monolithic operational amplifier, internally compensated for unity-gain stability.

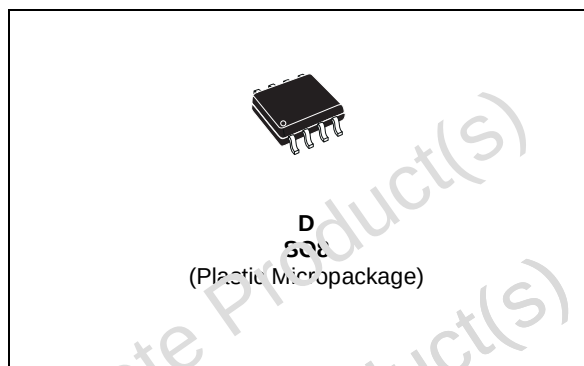
Low noise and low distortion, wide bandwidth and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

The TSH150 has internal electrostatic discharge (ESD) protection circuits and fulfills MILSTD883C-Class2.

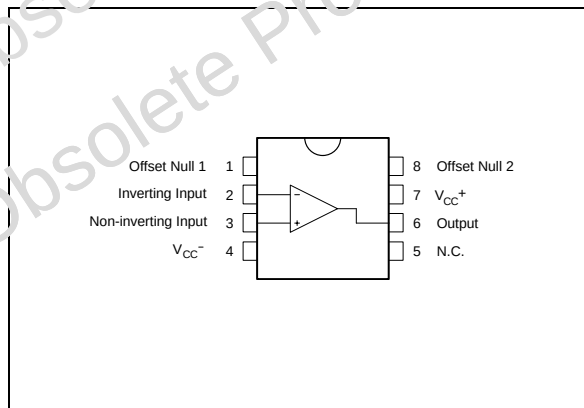
ORDER CODE

Part Number	Temperature Range	Package
		D
TSH150I	-40°C, +125°C	•

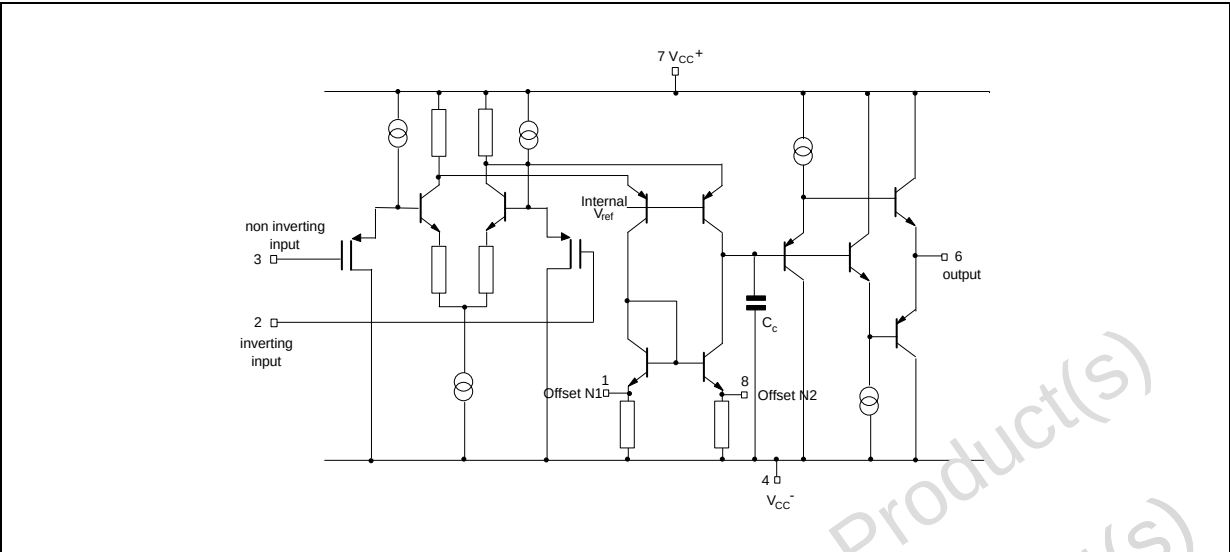
D = Small Outline Package (SO) - also available in Tape & Reel (DT)



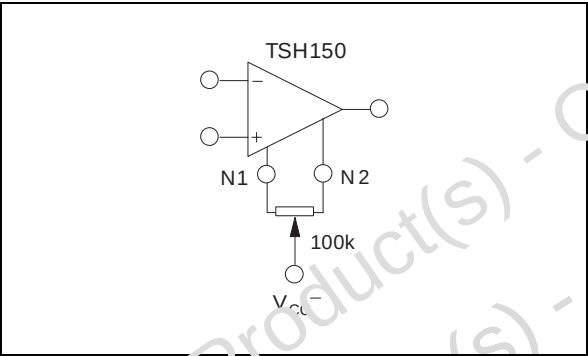
PIN CONNECTIONS (top view)



SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUIT



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 7	V
V_{id}	Differential Input Voltage	± 5	V
V_i	Input Voltage	± 5	V
I_{in}	Current On Inputs Current On Offset Null Pins	± 50 ± 20	V
T_{oper}	Operating Free-Air Temperature range	-40 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 3 to ± 6	V
V_{ic}	Common Mode Input Voltage Range	$V_{CC}^- + 2$ to $V_{CC}^+ - 1$	V

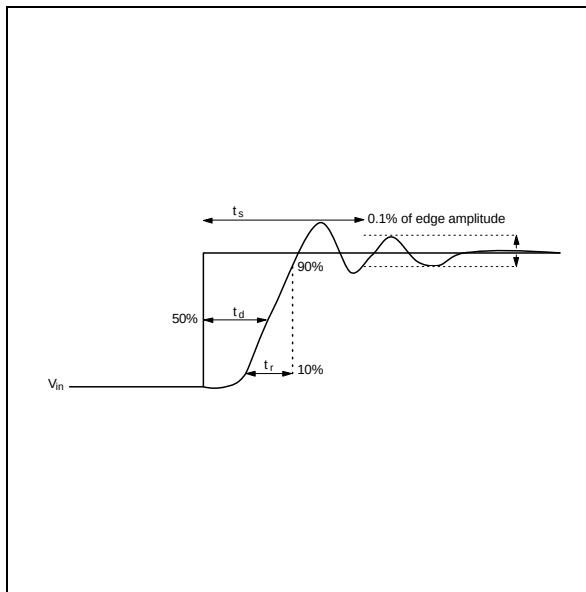
ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 5V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage $T_{min} \leq T_{amb} \leq T_{max}$		0.3	5 7	mV
DV_{io}	Input Offset Voltage Drift $T_{min} \leq T_{amb} \leq T_{max}$		10		$\mu V/^{\circ}C$
I_{ib}	Input Bias Current		5	30	μA
I_{io}	Input Offset Current		0.1	2	μA
I_{CC}	Supply Current, no load $V_{CC} = \pm 5V$ $V_{CC} = \pm 3V$ $V_{CC} = \pm 6V$ $T_{min} \leq T_{amb} \leq T_{max}$ $V_{CC} = \pm 5V$		23 21 25	30 28 40 37	mA
A_{vd}	Large Signal Voltage Gain $V_o = \pm 2.5V$ $R_L = \infty$ $R_L = 100\Omega$ $R_L = 50\Omega$	800 300 200	1300 850 650		V/V
V_{icm}	Input Common Mode Voltage Range	-3 to +4	3.5 to +4.5		V
CMR	Common-mode Rejection Ratio $V_{ic} = V_{icm \text{ min.}}$	60	100		dB
SVR	Supply Voltage Rejection Ratio $V_{CC} = \pm 5V$ to $\pm 3V$	50	70		dB
V_o	Output Voltage $R_L = 100\Omega$ $R_L = 50\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 100\Omega$ $R_L = 50\Omega$	± 3 ± 2.8 ± 2.9 ± 2.7	+3.5 -3.7 +3.3 -3.5		V
I_o	Output Short Circuit Current $V_{id} = \pm 1V$, $V_o = 0V$	± 50	± 100		mA
GBP	Gain Bandwidth Product $A_{VCL} = 10$, $R_L = 100\Omega$, $C_L = 15pF$, $f = 7.5MHz$		150		MHz
SR	Slew Rate $V_{in} = \pm 2V$, $A_{VCL} = 1$, $R_L = 100\Omega$, $C_L = 15pF$	100	190		V/ μs
e_n	Equivalent Input Voltage Noise $R_s = 50\Omega$ $f_o = 1kHz$ $f_o = 10kHz$ $f_o = 100kHz$ $f_o = 1MHz$		7 6.5 6.2 5.5		nV/ $\sqrt{Hz}$
K_{ov}	Overshoot $V_{in} = \pm 2V$, $A_{VCL} = 1$, $R_L = 100\Omega$, $C_L = 15pF$		5		%
t_s	Settling Time 0.1% ¹⁾ $V_{in} = \pm 1V$, $A_{VCL} = -1$		20		ns
t_r , t_f	Rise and Fall Time (see note 1) $V_{in} = \pm 100mV$, $A_{VCL} = 2$		3.5		ns
t_d	Delay Time (see note 1) $V_{in} = \pm 100mV$, $A_{VCL} = 2$		2.5		ns
ϕ_m	Phase Margin $A_{VM} = 1$, $R_L = 100\Omega$, $C_L = 15pF$		50		Degrees
THD	Total Harmonic Distortion $A_{VCL} = 10$, $f = 1kHz$, $V_o = \pm 2.5V$, no load		0.02		%
FPB	Full Power Bandwidth ²⁾ $V_o = 5V_{pp}$, $R_L = 100\Omega$ $V_o = 2V_{pp}$, $R_L = 100\Omega$		12 30		MHz

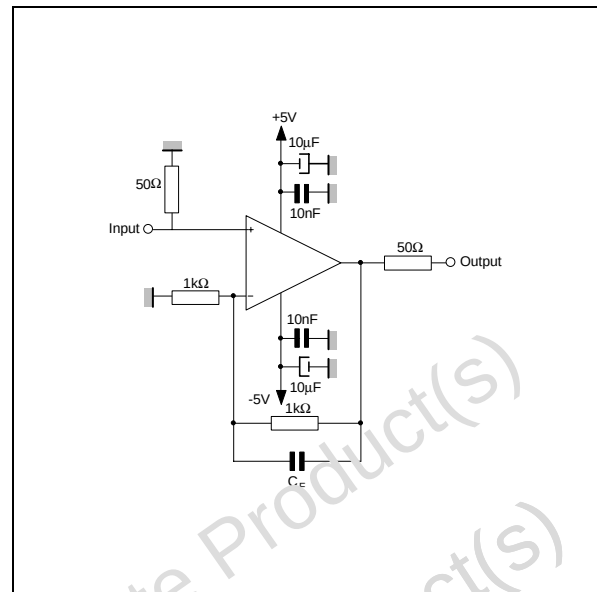
1. See test waveform figure

2. Full power bandwidth = $\frac{SR}{\pi V_{opp}}$

TEST WAVEFORM



EVALUATION CIRCUIT



PRINTED CIRCUIT LAYOUT

As for any high frequency device, a few rules must be observed when designing the PCB to get the best performances from this high speed op amp.

From the most to the least important points :

- ❑ Each power supply lead has to be bypassed to ground with a 10nF ceramic capacitor very close to the device and a 10μF tantalum capacitor.
- ❑ To provide low inductance and low resistance common return, use a ground plane or common point return for power and signal.
- ❑ All leads must be wide and as short as possible especially for op amp inputs. This is in

order to decrease parasitic capacitance and inductance.

- ❑ Use small resistor values to decrease time constant with parasitic capacitance.
- ❑ Choose component sizes as small as possible (SMD).
- ❑ On output, decrease capacitor load so as to avoid circuit stability being degraded which may cause oscillation. You can also add a serial resistor in order to minimise its influence.
- ❑ One can add in parallel with feedback resistor a few pF ceramic capacitor C_F adjusted to optimize the settling time.

MACROMODEL**Applies to: TSH150I**

** Standard Linear Ics Macromodels, 1993.

** CONNECTIONS :

* 1 INVERTING INPUT

* 2 NON-INVERTING INPUT

* 3 OUTPUT

* 4 POSITIVEPOWER SUPPLY

* 5 NEGATIVE POWER SUPPLY

.SUBCKT TSH150 1 3 2 4 5 (analog)

.MODEL MDTH D IS=1E-8 KF=1.568191E-15
CJO=10F

* INPUT STAGE

CIP 2 5 1.000000E-12

CIN 1 5 1.000000E-12

EIP 10 5 2 5 1

EIN 16 5 1 5 1

RIP 10 11 1.040000E+02

RIN 15 16 1.040000E+02

RIS 11 15 3.264539E+02

DIP 11 12 MDTH 400E-12

DIN 15 14 MDTH 400E-12

VOFP 12 13 DC -9.162265E-05

VOFN 13 14 DC 0

IPOL 13 5 1.000000E-03

CPS 11 15 5.757255E-12

DINN 17 13 MDTH 400E-12

VIN 17 5 1.500000E+00

DINR 15 18 MDTH 400E-12

VIP 4 18 0.500000E+00

FCP 4 5 VOFP 2.200000E+01

FCN 5 4 VOFN 2.200000E+01

FIBP 2 5 VOFP 1.000000E-02

FIBN 5 1 VOFN 1.000000E-02

* AMPLIFYING STAGE

FIP 5 19 VOFP 4.370000E+02

FIN 5 19 VOFN 4.370000E+02

RG1 19 5 1.124121E+03

RG2 19 4 1.124121E+03

CC 19 29 2.000000E-09

HZTP 30 29 VOFP 5.574976E+01

HZTN 5 30 VOFN 5.574976E+01

DOPM 19 22 MDTH 400E-12

DONM 21 19 MDTH 400E-12

HOPM 22 28 VOUT 5.000000E+02

VIPM 28 4 5.000000E+01

FCNM 21 27 VOUT 5.000000E+02

VINM 5 27 5.000000E+01

EOUT 26 23 19 5 1

VOUT 23 5 0

ROUT 26 3 2.180423E+01

COUT 3 5 1.000000E-12

DOP 19 25 MDTH 400E-12

VOP 4 25 1.511965E+00

DON 24 19 MDTH 400E-12

VON 24 5 1.511965E+00

.ENDS

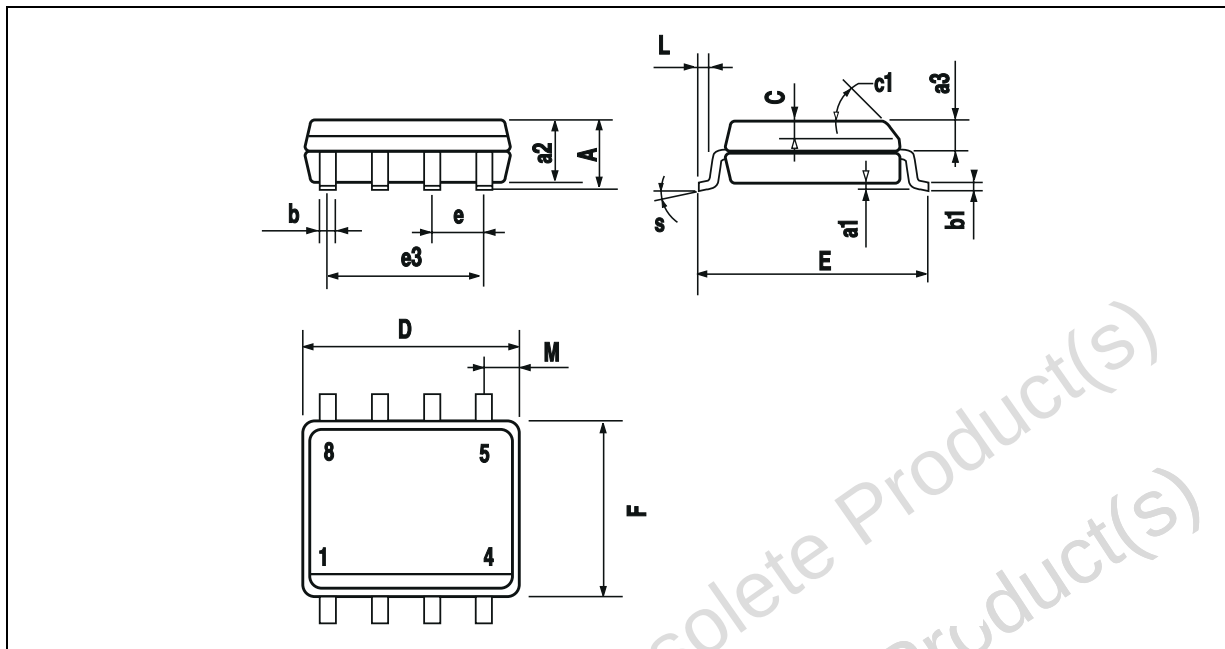
ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 5V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	$R_L = 100\Omega$	1	V/mV
I_{CC}	No load	21	mA
V_{icm}		-3.5 to 4.5	V
V_{OH}	$R_L = 100\Omega$	+3.6	V
V_{OL}	$R_L = 100\Omega$	-3.6	V
I_{sink}	$V_o = 0V$	108	mA
I_{source}	$V_o = 0V$	108	mA
GBP	$R_L = 100\Omega$, $C_L = 15pF$	147	MHz
SR	$R_L = 100\Omega$, $C_L = 15pF$	180	V/ μs
ϕ_m	$R_L = 100\Omega$, $C_L = 15pF$	42	Degrees
t_s	$A_v = -1$ at 0.1%	22.6	ns

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC MICROPACKAGE (SO)



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1			45° (typ.)			
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S			8° (max.)			

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2000 STMicroelectronics - Printed in Italy - All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>